REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-12, 14-18, and 20 are pending in this application. Claim 13 is canceled by the present response without prejudice, claim 19 having previously been canceled without prejudice. Claim 13 was objected to under 37 C.F.R. § 1.75(c). Claims 1-20 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent 4,663,644 to Shimizu.

Initially, applicant and applicants' representative wish to thank Examiner Cao for the interview granted applicants' representative on January 9, 2006. During the interview the outstanding rejections were discussed in detail. Further, during the interview claim amendments to clarify claimed features were also discussed. The present response submits the discussed claim amendments and reiterates comments presented during the interview as to the allowability of the claims over the applied art. Examiner Cao indicated such claim amendments appear to address the current rejections.

Addressing first the objection to claims 13, that objection is obviated by the present response as claim 13 is canceled by the present response.

Addressing now the rejection of claims 1-20 under 35 U.S.C. § 102(b) as anticipated by Shimizu, that rejection is traversed by the present response.

Each of the independent claims is amended by the present response to clarify features recited therein. Specifically, independent claim 1 now clarifies the first gate insulating film is formed "on both of sidewall-surfaces opposed to each other" of the first electrode group. Independent claim 1 now additionally recites "a channel region formed along the gate insulating film on both of the sidewall-surfaces opposed to each other of the first gate electrode of the first gate electrode group". The other independent claims now also recite similar features. No new matter is believed to be added by the amendments.

With the claimed structure, as the first gate insulating film is not formed only on the main sidewall surface, but is also formed on the other sidewall surface opposed to the main sidewall surface, a channel region is formed on both of the sidewall surface regions in the semiconductor device. As shown in Figure 8 in the present specification as a non-limiting example, a gate insulating film 16 is formed on both sides of the poly-silicon film 17 for a gate electrode. Thereby, channel regions 25 can be induced along both of the sidewall-surface regions in the silicon layers 13 along the gate insulating film 16. As a result, an area of a channel region in the semiconductor device of the claimed invention can be significantly increased. Further, since a greater number of channel regions can be formed in a given area with a minimum design space, a channel density can be increased, and the device resistance for a MOSFET can be lowered.

Applicants respectfully submit Shimizu does not disclose or suggest the claimed structure.

The outstanding Office Action relies upon the gate insulating film 2 in Shimizu to meet the limitations of the claimed "first gate insulating film". However, in that respect applicants note film 2 is only formed on the first main sidewall surface and a bottom surface of the gate electrode of a pair of the MOSFETs in Shimizu. That is, that insulating film 2 is not formed on both of the sidewall surfaces that are opposed to each other of a gate electrode. In Shimizu a different film 5 opposes the film 2.

In maintaining the outstanding rejection, the Advisory Action of December 13, 2005 now appears to indicate that film 5 is a portion of the gate insulating film 2 "because it is used to insulate between the adjacent gate electrodes 4a (see Fig. 1 and column 5, lines 2-5)".

Applicants respectfully further traverse that position on the following grounds.

First, applicants note Shimizu only discloses the gate insulating film 2 acting as a gate for a channel in a semiconductor layer 10. Shimizu fails to disclose the insulating film 5 as a

gate insulating film. Applicants respectfully submit the insulating film 5 only acts as an insulator between two gate electrodes 4a.

Moreover, the claims now further distinguish over such an interpretation in Shimizu. Independent claim 1 recites "a channel region formed along the gate insulating film on both of the sidewall-surfaces opposed to each other of the first gate electrode of the first electrode group"; and as similar recited in the other independent claims. For Shimizu to meet that limitation, Shimizu would have to have a structure in which a channel region was formed along both the gate insulating film 2 and the film 5. However, applicants respectfully it is clearly not the case that in Shimizu the channel region is formed along both the films 2 and 5.

In contrast to Shimizu, and with reference to Figure 8 in the present specification as a non-limiting example, a channel region 25 is formed along both of the sidewall-surfaces opposed to each other of the gate insulating film 16. Shimizu does not disclose that structure. In Shimizu a channel is formed only in the silicon layer adjacent to the gate insulating film 2, but is not formed along the gate insulating film 5.

In view of these foregoing comments, the claims as currently written are believed to clearly distinguish over the applied art to Shimizu.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is herby respectfully requested that this case be passed to issue.

Respectfully submitted,

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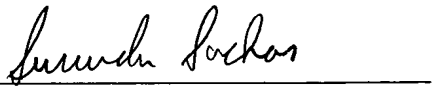
MAIER & NEUSTADT, P.C.



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